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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,614	11/24/2003	Martin G. Rammel	BO1-0162US	4243

60483 7590 09/27/2007

LEE & HAYES, PLLC
421 W. RIVERSIDE AVE.
SUITE 500
SPOKANE, WA 99201

EXAMINER	
DAO, THUY CHAN	
ART UNIT	**PAPER NUMBER**
2192	

MAIL DATE	DELIVERY MODE
09/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/720,614	RAMMEL, MARTIN G.	
	Examiner	Art Unit	
	Thuy Dao	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9,12-21,24-25,27-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9,12-21,24-25,27-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the amendment filed on July 19, 2007.

2. Claims 1-7, 9, 12-21, 24-25, and 27-30 have been examined.

Response to Amendments

3. Per Applicant's request, claims 1, 4-5, 13-15, and 19 have been amended; claims 8, 10-11, 22-23, and 26 have been canceled; and claims 27-30 have been added.

4. The objection to the specification is withdrawn in view of Applicant's amendments.

Response to Arguments

5. The Applicant is thanked for a thorough reply. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Drawings

6. The drawings are objected to. In figure 1, out port "24" should be - -26- -.

Applicant's arguments appear to direct to Figure 1 originally filed November 24, 2003. The examiner would like to direct the Applicant to Figure 1, amended December 17, 2004, which has a wrong reference number "24", instead of - -26- -.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

7. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

In the instant case, the phrase in lines 1-2 is considered to read as - -[[Apparatus and methods for improving ... are disclosed. In one embodiment, a]] A method of performing ...- -.

Appropriate correction is required.

Claim Objections

8. Claims 3 and 16 are objected to because of minor informalities: acronyms VHDL, FPGA, and FFT should be spelled out at the first appearance in claims.

9. Claim 7 is objected to. The phrase in line 3 should be - -adapted to [[deliniate]] delineate the portions ...- -.

10. Claim 9 is objected to because of minor informalities. The phrase is considered to read as - -[[(Original)]] (Currently Amended) The method of Claim [[8]] 1 ...- -.

11. Claims 27-30 are objected to because of minor informalities. The Applicant added claims 27-30 without pointing out the supporting text in the originally filed disclosure. For a proper prosecution record, the examiner respectfully requests the Applicant point out the supporting text for newly added limitations in the next communications with the Office to obviate a potential 35 USC 112 paragraph rejection.

Appropriate correction is required.

Claim Rejections – 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 1-7, 9, 12-21, 24-25, and 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cantle (art of record, "A Foundation Architecture For Elevating DSP in FPGAs") in view of US Patent No. 6,163,836 to Dowling (art made of record, hereinafter "Dowling").

Claim 1:

Cantle discloses *a method of performing a numerical simulation, comprising:*

a programmable device (e.g., page 6, Figure 5, FPGA component);

receiving input data (e.g., Figure 5, DIME I/O Connector, lines 14-16);

routing a first portion of the received input data to a processor (e.g., page 6: 12-17, DSP sharing floating point computing; page 2, FIG. 2, routing a first portion to DSP as a coprocessor, emphasis added);

routing a second portion of the received input data to the programmable device (e.g., page 2, FIG. 2, routing a second portion to FPGA as main processor; page 5, FIG. 5 and related text);

performing a first portion of the numerical simulation on the processor using the first portion of the received input data (e.g., Figure 5, SHARC digital signal processor DSP, lines 16-20);

performing a second portion of the numerical simulation on the programmable device using the second portion of the received input data (e.g., page 6, one million gate FPGA);

combining the results of the first and second portions of the numerical simulation; and outputting the combined results (e.g., page 2, FIG. 2 and related text, Data Out; page 6, FIG. 5, inputting parallel digital video, sharing the floating point computing, and outputting the combined pixel manipulations).

Cantle discloses a FPGA as a programmable device but does not explicitly disclose *programming a programmable device using a plurality of function blocks.*

However, in an analogous art, Dowling discloses *generating a plurality of VHDL function blocks and programming a programmable device using a plurality of function blocks* (e.g., col.5: 31-45; col.15: 12-24; col.15: 66 – col.16: 31; col.16: 56 – col.17: 9).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine the teaching of Dowling into that of Cantle. One would have been motivated to do so to because said FPGA is programmable and re-programmable (FPGA stands for Field Programmable Gate Array) by using synthesis tools and allow programmer to implement very complex address calculation algorithms as suggested by Dowling (e.g., col.15: 12-24; col.16: 32-44; col.16: 56 – col.17:9).

Claim 2:

The rejection of claim 1 is incorporated. Dowling also discloses *generating a plurality of function blocks* as set forth in claim 1 above.

Claim 3:

The rejection of claim 2 is incorporated. Dowling also discloses *generating a plurality of function blocks includes generating a plurality of VHDL function blocks* (e.g., col.15: 12-24; col.16: 56 – col.17: 9).

Claim 4:

The rejection of claim 1 is incorporated. Cantle also discloses *exchanging data from at least one of the first and second portions via the data path includes providing inputs to a simulation block programmed into the programmable device from the processor via the data path* (e.g., page 6, FIG. 5 and related text, I/O Connectors, Parallel Communications Links, SDRAM of FPGA).

Claim 5:

The rejection of claim 1 is incorporated. Cantle also discloses *exchanging data from at least one of the first and second portions via the data path includes providing outputs from a simulation block programmed into the programmable device to the processor via the data path* (e.g., page 6, FIG. 5, tow Sharc DSPs with SSRAM directly connected for parameter passing and synchronization).

Claim 6:

The rejection of claim 1 is incorporated. Cantle also discloses *performing a second portion of the numerical simulation on the programmable device includes performing a portion of the original simulation on the programmable device* (e.g., page 2, FIG. 2 and related text, Data In and sharing portion in main processor FPGA with other portions from coprocessor DSP).

Claim 7:

The rejection of claim 6 is incorporated. Cantle also discloses *performing a portion of the simulation on the programmable device includes: receiving inputs into a pair of gateway in blocks adapted to delineate the portions of the simulation to convert*

into VHDL for operation in hardware (e.g., page 5, FIG. 4 and related text, dynamically reconfiguring FPGA in DIME system).

Claim 9:

The rejection of claim 1 is incorporated. Cantle also discloses *performing a portion of a simulation on the programmable device includes: coupling the outputs of the portion of the simulation to be run in hardware to at least one gateway out block adapted to delineate the extent of the code to be converted into VHDL for execution in hardware* (e.g. page 7, FIG. 6 and related text, processing analogue video on hardware module BallyBlue and Ballyvision).

Claim 12:

The rejection of claim 1 is incorporated. Cantle also discloses *forming a synthesis of the function blocks; and synthesizing a file adapted for use to program gate connections of the programmable device* (e.g., page 5, FIG. 4, Session Log, synthesizing a Bit File to module 2 of Xlinx Virtex SCV300).

Claims 13-15:

Claims 13-15 recite the same limitations as those of claims 1-5, wherein all claimed limitations have been addressed and/or set forth above. Therefore, as the reference teaches all of the limitations of the above claims, it also teaches all of the limitations of claims 13-15.

Claim 16:

The rejection of claim 13 is incorporated. Cantle also discloses *programming a programmable device includes programming an FPGA device using at least some VHDL function blocks, and wherein performing a second portion of the numerical simulation on the programmable device includes performing an FFT on the programmable device* (e.g., pp. 1-2, elevating DSP in FPGA by performing HWIL).

Claim 17:

The rejection of claim 16 is incorporated. Cantle also discloses limitations in claim 17 (e.g., pp. 7-8, modules to process complex two dimensional images, analogue video).

Claim 18:

The rejection of claim 13 is incorporated. Cantle also discloses *forming a synthesis of the function blocks; and synthesizing a file adapted for use to program gate connections of the programmable device* (e.g., page 5, FIG. 4 and related text, synthesizing a Bit File to module).

Claim 19:

Cantle discloses *an apparatus for performing a numerical simulation, comprising:*

an input device adapted to receive input data (e.g.. page 2, FIG. 2, Data In to FPGA main processor; page 6, FIG. 5 and related text, receiving parallel digital video)*;*

a processor (e.g., page 2 and page 6, DSPs as coprocessors)*;*

a programmable device and a module (e.g., page 2 and page 6, FPGAs as main processors and module)*, wherein:*

the module routs a first portion of the received input data to the processor and routs a second portion of the received input data to the programmable device (e.g., FIG. 5 and related text, main processor FPGA using parallel communications links to share floating point computing)*;*

the processor is adapted to perform a first portion of the numerical simulation using the first portion of the received input data (e.g., page 6, two Sharc DSPs performing the shared floating point computing from main processor FPGA)*;*

the programmable device is adapted to perform a second portion of the numerical simulation, using the second portion of the received input data (e.g., FIG. 2 and FIG. 5, main processor FPGA performing a second portion of computing)*; and*

the module combines the results of the first and second portions of the numerical simulation (e.g., page 2 and page 6, DIME I/O Connector, Data Out as the output pixel manipulations of the parallel digital video).

Cantle discloses a FPGA as a programmable device but does not explicitly disclose *the programmable device is adapted to use at least some function blocks.*

However, in an analogous art, Dowling discloses *programming a plurality of VHDL function blocks and using at least some function blocks* (e.g., col.5: 31-45; col.15: 12-24; col.15: 66 – col.16: 31; col.16: 56 – col.17: 9).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine the teaching of Dowling into that of Cantle. One would have been motivated to do so to because said FPGA is programmable and re-programmable (FPGA stands for Field Programmable Gate Array) by using synthesis tools and allow programmer to implement very complex address calculation algorithms as suggested by Dowling (e.g., col.15: 12-24; col.16: 32-44; col.16: 56 – col.17:9).

Claim 20:

The rejection of claim 19 is incorporated. Dowling further discloses *a generator adapted to generate a plurality of function blocks, at least some of the function blocks being adapted to perform a respective part of the second portion of the numerical simulation* (e.g., col.15: 66 – col.16: 31; col.16: 56 – col.17: 9).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine the teaching of Dowling into that of Cantle. One would have been motivated to do so to as set forth above.

Claim 21:

The rejection of claim 20 is incorporated. Dowling further discloses *the generator is further adapted to generate a plurality of VHDL function blocks* as in claim 20 above.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine the teaching of Dowling into that of Cantle. One would have been motivated to do so to as set forth above.

Claim 24:

The rejection of claim 19 is incorporated. Dowling further discloses *the programmable device is further adapted to perform a simulation function block* (e.g., col.5: 31-45; col.15: 12-24).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine the teaching of Dowling into that of Cantle. One would have been motivated to do so to as set forth above.

Claim 25:

The rejection of claim 24 is incorporated. Cantle also discloses *the programmable device is further adapted to: receive inputs into a pair of gateway in* (e.g., page 7, FIG. 6 and related text).

Claim 27 (new):

The rejection of claim 1 is incorporated. Cantle also discloses *routing a second portion of the received input data to the programmable device comprises selecting the most time consuming portion of the numerical simulation to be routed to the programmable device* (e.g., pages 1-2, traditional hardware architecture changes to FPGA Central, which processes time consuming portions).

Claim 28 (new):

The rejection of claim 1 is incorporated. Cantle also discloses *selecting the most time consuming portion of the numerical simulation comprises selecting a portion of the numerical simulation that includes at least one logical operation* (e.g., page 2, lines 1-10).

Claims 29-30 (new):

Claims 29-30 recite the same limitations as those of claims 27-28, wherein all claimed limitations have been addressed and/or set forth above. Therefore, as the reference teaches all of the limitations of the above claims, it also teaches all of the limitations of claims 29-30.

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

15. Any inquiry concerning this communication should be directed to examiner Thuy Dao (Twee), whose telephone is (571) 272 8570. The examiner can normally be reached on every Tuesday, Thursday, and Friday from 6:00AM to 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam, can be reached at (571) 272 3695.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273 8300.

Any inquiry of a general nature of relating to the status of this application or proceeding should be directed to the TC 2100 Group receptionist whose telephone number is (571) 272 2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

T. Dao

TUAN DAM
SUPERVISORY PATENT EXAMINER